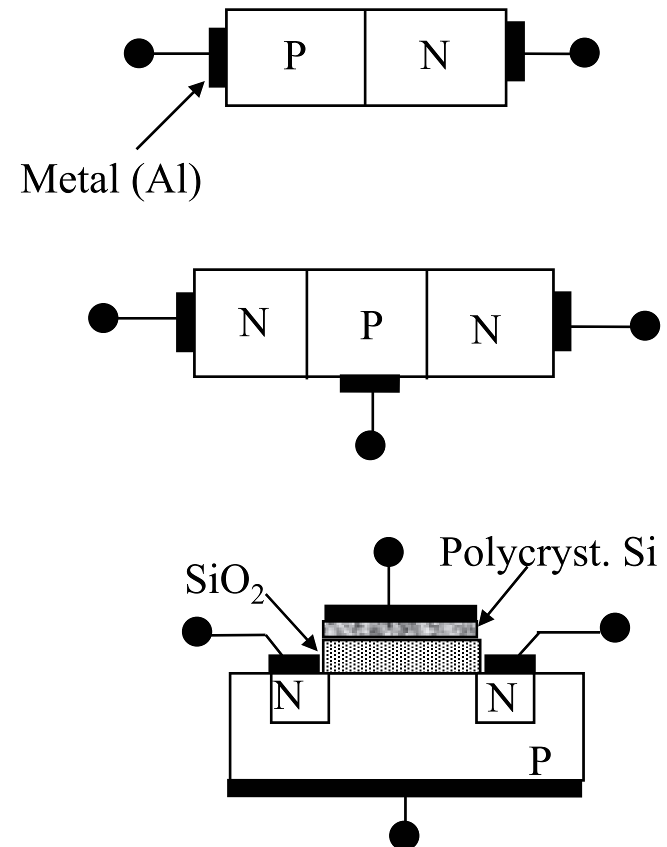
Fabrication Technology, Part I

- Agenda:
  - Microfabrication—Overview
    - Basic semiconductor devices
    - Materials
    - Key processes
  - Oxidation
  - Thin-film Deposition

Reading: Senturia, Ch. 3 pp. 29-44.

Basic Semiconductor Devices

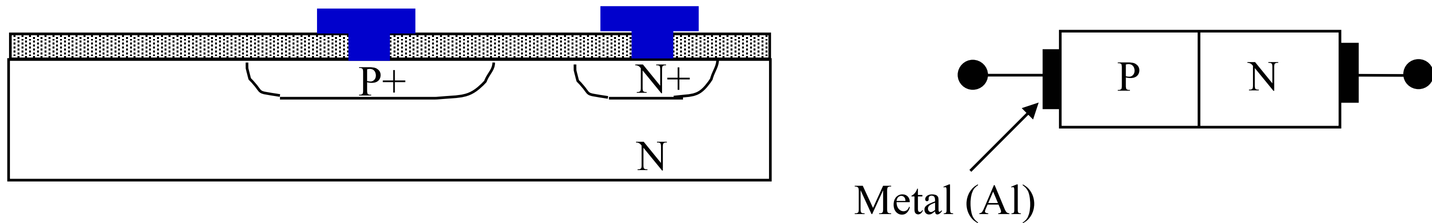
- P/N diode
- Bipolar junction transistor (BJT)
  - N/P/N
  - P/N/P
- Metal-oxide-semiconductor field-effect transistor (MOSFET)
  - n-channel (NMOS)
  - p-channel (PMOS)
  - complementary MOS (CMOS)



Basic Semiconductor Devices

- **Diode**

Planar Process



- **CMOS**

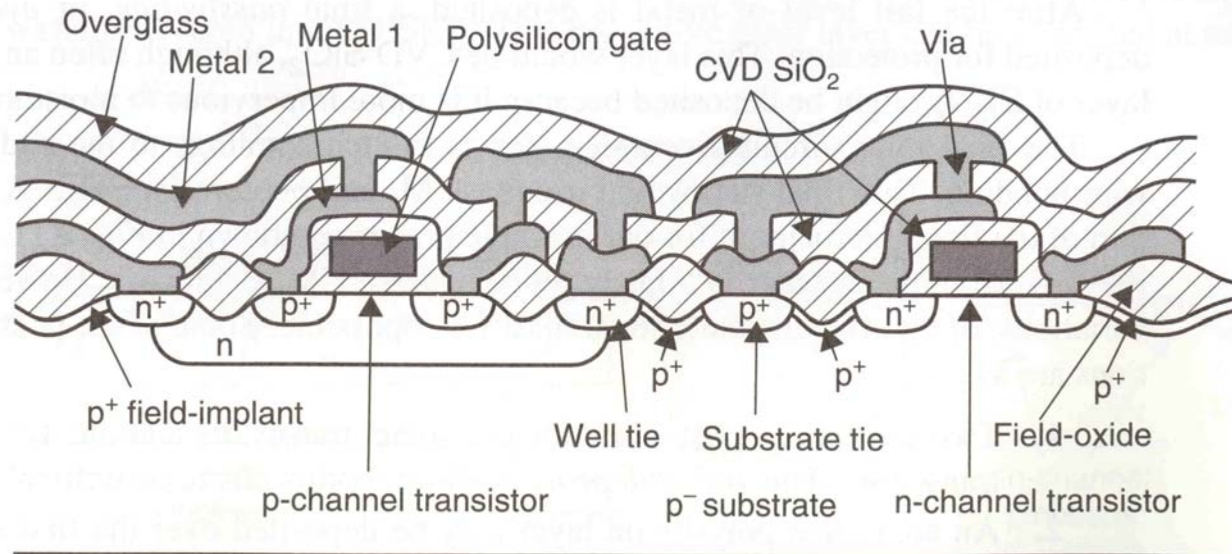
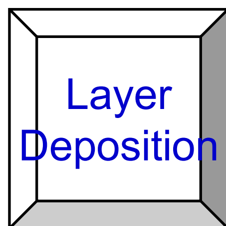


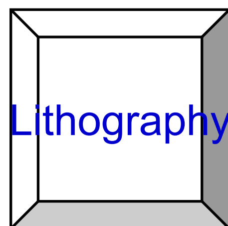
Fig. 2.11 Final cross section of an example CMOS microcircuit.

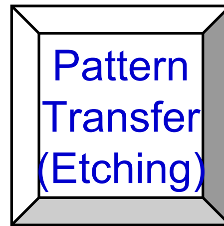
Johns and Martin, *Analog Integrated Circuit Design*

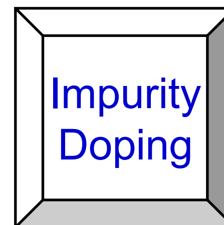
Microfabrication--Overview

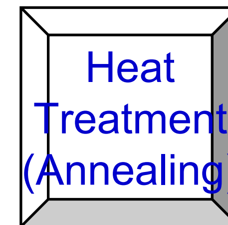
- Microfabrication
  - Silicon integrated circuit fabrication
  - > 40 years of collective equipment and process experience
  - Primarily planar process
  - Key processes:











Layer Deposition	Lithography	Pattern Transfer (Etching)	Impurity Doping	Heat Treatment (Annealing)
Growth Physical Chemical	Contact Projection	Wet Dry (Plasma, RIE)	Ion implant Solid source	Furnace RT

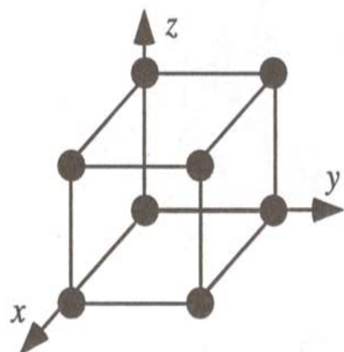
Substrate Materials

- Group IV Elemental Semiconductors
  - 4 valence electrons
  - tetrahedral bonding
  - diamond crystal lattice
- Group III-V Compound Semiconductors
  - Optical devices
  - High speed
  - Wide band-gap, narrow band-gap
- Silicon
  - Dominant semiconductor
  - Intermediate temperature operation
  - Superior grown insulator, SiO_2

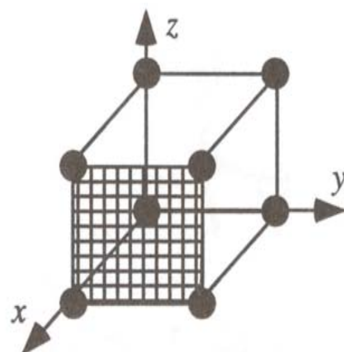
III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb
Tl	Pb	Bi

Host (arrow pointing to column IV)

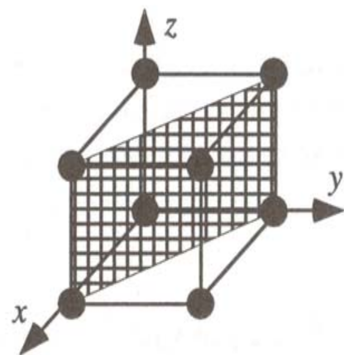
Miller Index



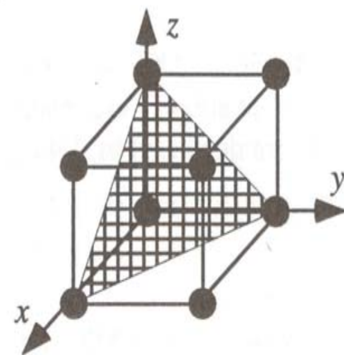
Simple cubic crystal



(100) plane



(110) plane



(111) plane

Illustrating the different major crystal planes for a simple cubic lattice of atoms.

To find the miller index of a plane:

Step 1: Find intersection of plane

Step 2: Take reciprocal

Step 3: Reduce to lowest common integer

Notation for Miller indices

(ijk): a specific crystal plane or face

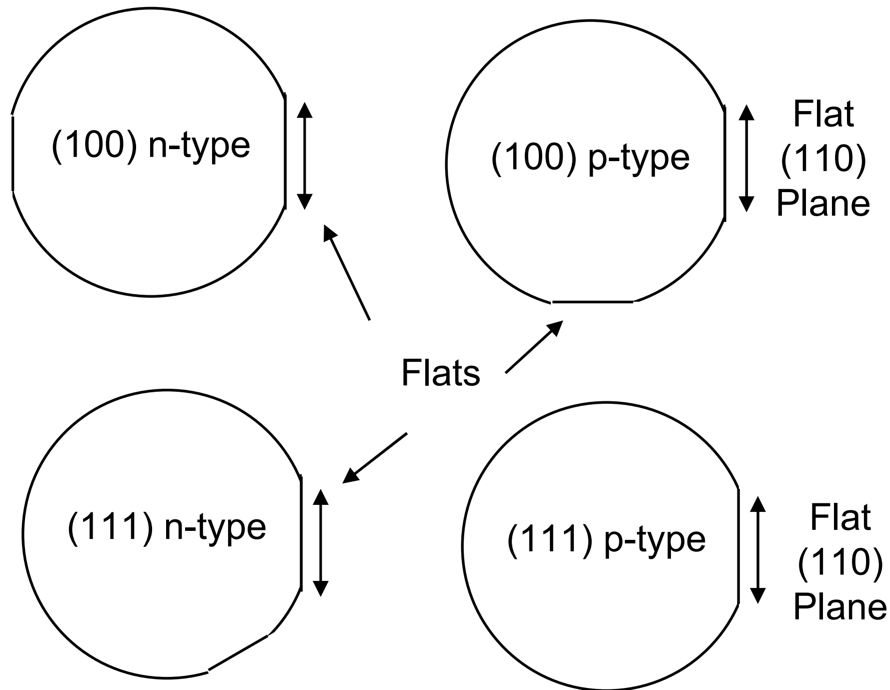
{ijk}: a family of equivalent planes

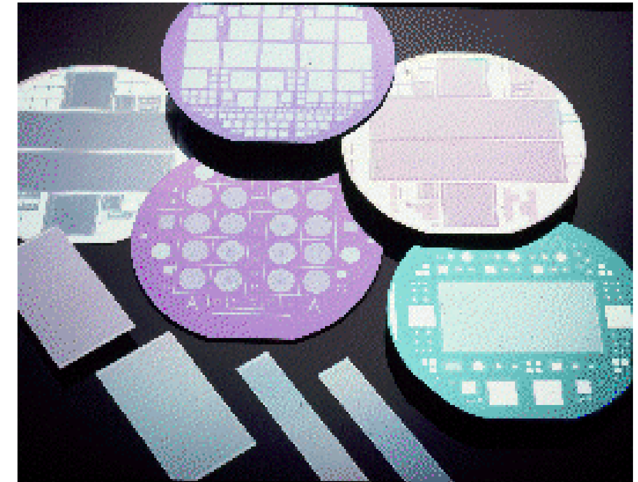
[ijk]: a specific direction which is normal to the (ijk) plane

<ijk>: a family of equivalent directions

Substrate Materials: Silicon

- Defined by plane crystal orientation and wafer flat direction





N-type Silicon

- Group V Impurities
  - 5 valence electrons
  - 4 valence electrons form covalent bonds with 4 nearest neighbor valence electrons
    - Extra electron 'donated' if $kT > E_i = 44$ meV (fully ionized at R.T.)
- N-type semiconductor
  - Semiconductor with intentionally added concentration of group V impurity, N_D
  - Electron-rich

    $N \cong N_D > P$

    - where N=conduction electron concentration and P=valence hole concentration (units: $\#/cm^3$)

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb
Tl	Pb	Bi

Host (IV) — Donor 'n-type' (V)

P-type Silicon

- Group III Impurities
  - 3 valence electrons
  - 3 valence electrons form covalent bonds with 3 nearest neighbors, 1 incomplete
    - Results in hole that is ionized if kT > E_I= 45 meV (fully ionized at R.T.)
- P-type semiconductor
  - Semiconductor with intentionally added concentration of group III impurity, N_A
  - Hole-rich

    $P \cong N_A > N$

    - where N=conduction electron concentration and P=valence hole concentration (units: #/cm^3)

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb
Tl	Pb	Bi

Acceptor 'p-type' (column III) — Host (column IV)

Layer Deposition--Oxidation

- Oxidation of Silicon (SiO_2)
  - Best natural insulator
  - SiO_2 Properties
    - As grown, amorphous
    - Melting point 1600°C
    - Density 2.2 g/cm^3
    - Refractive index 1.46
    - Dielectric strength, approx. 10^7 V/cm
    - Energy gap, approx. 9 eV
    - Thermal expansion coeff. 5×10^{-7}/C
    - Thermal conductivity 0.014 W/cm-K
    - DC resistivity at 25°C approx. 10^{14}-10^{16} $\Omega \cdot$cm

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Oxidation

- Principal Uses
  - Insulating layer in device and between metal lines
  - Passivation layer to seal silicon surface
  - Blocking layer to stop or mask impurity atoms
- Thickness Ranges
  - 25(?)-1000Å Gate Oxides
  - 2000-5000 Å Masking Oxides
  - 3000-10000 Å Field Oxides

Oxidation Kinetics

- Thermal Oxidation
  - Si(s) + O_2(g) --> SiO_2(s) (dry)
  - Si(s) + 2H_2O(g) --> SiO_2(s) + 2H_2(g) (wet)
- Reaction
  - Gas phase transport of oxidation species to silicon surface
    - Diffusion through existing oxide
    - Reaction at silicon surface
  - Silicon consumed to make SiO_2

$$x_{Si} = 0.46x_{ox}$$

  - Deal-Grove Model

B/A = linear rate coefficient

B = parabolic rate constant

x_i=initial oxide thickness

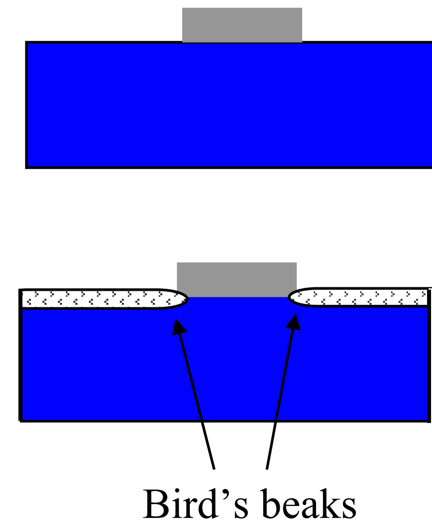
$$x_{ox} = 0.5A\left(\sqrt{1+\frac{4B}{A^2}(t+\tau)}-1\right)$$

$$\tau = \frac{x_i^2}{B} + \frac{x_i}{(B/A)}$$

Thermal Oxidation -- Details

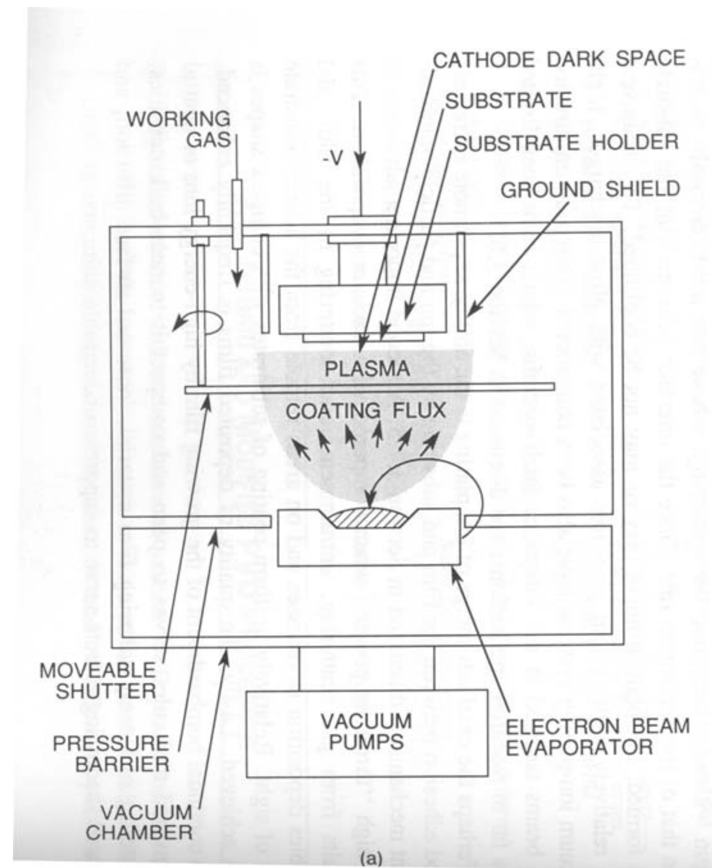
- Thermal Oxidation--Details
  - Dry Oxide
    - Denser oxide
    - Higher dielectric strength
    - Gate oxide for MOSFET (CMOS)
  - Wet Oxide
    - Faster growth
    - Field oxide
  - Dry/Wet/Dry process
    - High quality Si/SiO_2 interfacial oxide
    - Faster growth
  - Cleanliness essential
    - Oxide charge very detrimental

- **Local Oxidation of Silicon (LOCOS)**



Layer Deposition--Physical

- Thermal Evaporation
  - Sublimation of heated material in vacuum
    - Resistive or e-beam kinetic energy source
  - Limitations
    - metal selection
- Sputtering
  - Momentum transfer induces release of material via energetic Ar^+ ion impact
  - Limitations
    - Cost, bombardment damage
- Electron-beam evaporation
  - Metals
  - Dielectric materials (ZnO, Al_2O_3, SiO_2)



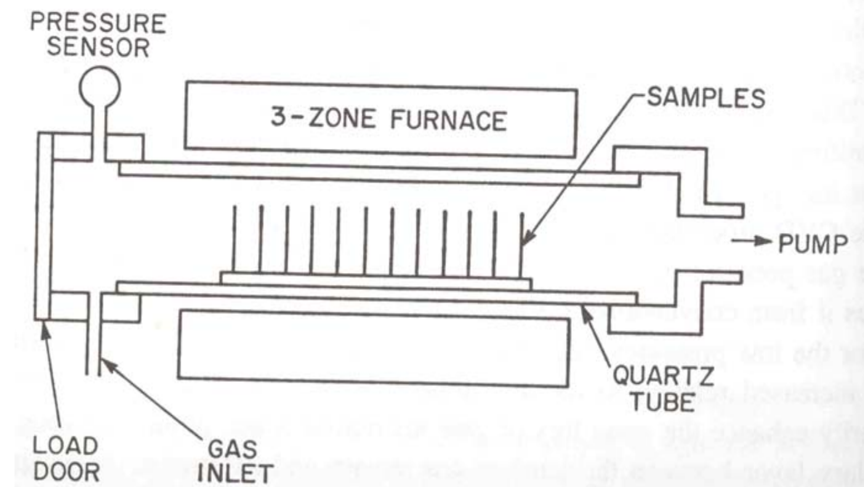
Layout Deposition--Chemical

Layer Deposition--Chemical

- Deposition Techniques
  - Atmospheric pressure (APCVD)
  - Low pressure (LPCVD)
  - Plasma-enhanced (PECVD)
  - Metal organic CVD (MOCVD)

- Deposition Variables
  - Substrate temperature
  - Pressure
  - Gas composition

- A schematic of a typical LPCVD reactor



Layer Deposition--Chemical

Material	Reaction	Temperature (°C)
SiO_2	$SiCl_2H_2 + 2N_2O \text{ --> } SiO_2 + 2N_2 + 2HCl$	850-900 (LP)
	$Si(OC_2H_5)_4 + 12O_2 \text{ --> } SiO_2 + 8CO_2 + 10H_2O$	650-750 (LP)
	$SiH_4 + O_2 \text{ --> } SiO_2 + 2H_2$	400-450 (AP)
	$SiH_4 + 4N_2O \text{ --> } SiO_2 + 4N_2 + 2H_2O$	200-350 (PE)
Si_xN_y	$3SiH_4 + 4NH_3 \text{ --> } Si_3N_4 + 12H_2$	700-900 (AP)
	$3SiCl_2H_2 + 4NH_3 \text{ --> } Si_3N_4 + 6HCl + 6H_2$	650-750 (LP)
	$SiH_4 + NH_3 \text{ --> } SiNH + 3H_2$	200-350 (PE)
Poly-Si	$SiH_4 \text{ --> } Si + 2H_2$	600-650 (LP)
W	$WF_6 + H_2 \text{ --> } W$ + by-products	580 (LP)

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Layer Deposition--Other

- Electroplating
  - Electrochemical process
  - Cu, Au, Cr, Ni, permalloy
  - Copper interconnect, microstructures
  - Low temperature
  - Rough surface; wet process; protection

- Sol-Gel deposition
  - Spin-on glasses
  - Piezoelectric materials
  - Low temperature

- Spin casting
  - Photoresist
  - Polyimide